Claims

What is claimed is:

1. A method for evaluating a digital signaling system comprising the steps of:

generating a transmit repeating pattern in a transmit circuit;

transmitting the transmit repeating pattern to a receive circuit;

generating a receive repeating pattern in the receive circuit;

comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison; and

adjusting a parameter affecting reception of the transmit repeating pattern at the receive circuit.

2. The method of claim 1 wherein the parameter is a termination setting.

3. The method of claim 1 wherein the parameter is a transmit clock offset.

4. The method of claim 1 wherein the parameter is a receive clock offset.

5. The method of claim 1 wherein the parameter is an input receiver window.

6. The method of claim 1 wherein the parameter is an output drive level.

7. The method of claim 1 wherein the parameter is a crosstalk cancellation coefficient.

8. The method of claim 1 wherein the parameter is an equalization coefficient.

9. The method of claim 1 wherein the step of generating a transmit repeating pattern in a transmit circuit comprises the step of:

utilizing a shift register to generate the transmit repeating pattern.

10. The method of claim 9 wherein the step of utilizing a shift register to generate the transmit repeating pattern comprises the step of:

utilizing a linear feedback shift register to generate the transmit repeating pattern.

11. The method of claim 1 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern as a signal referenced to a ground.

12. The method of claim 1 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern as a differential signal over a pair of conductors.

13. The method of claim 1 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously.

14. The method of claim 1 further comprising the step of:

setting the parameter affecting reception of the transmit repeating pattern at the receive circuit.

15. The method of claim 1 wherein the step of adjusting the parameter affecting reception of the transmit repeating pattern at the receive circuit is repeated over a range of values of the parameter.

16. The method of claim 15 wherein the steps of transmitting the transmit repeating pattern to the receive circuit and comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison are repeated after the step of adjusting the parameter affecting reception of the transmit repeating pattern at the receive circuit is performed.

17. The method of claim 16 further comprising the step of:

constructing a representation of a waveform based on the comparison.

18. The method of claim 1 further comprising the step of:

selecting a value of the parameter so as to optimize reception at the receive circuit of a transmit data output signal transmitted by the transmit circuit.

19. The method of claim 18 wherein the transmit repeating pattern and the transmit data output signal are communicated from the transmit circuit to the receive circuit over a common medium.

20. The method of claim 19 wherein the common medium is a data line.

21. The method of claim 19 wherein the common medium is an address line.

22. The method of claim 19 wherein the common medium is a control line.

23. The method of claim 18 wherein at least one medium is used to communicate the transmit data output signal is not used to communicate the transmit repeating pattern.

24. The method of claim 23 wherein the at least one medium is a data line.

25. The method of claim 23 wherein the at least one medium is an address line.

26. The method of claim 23 wherein the at least one medium is a control line.

27. The method of claim 23 wherein at least one analysis medium is used to communicate the transmit repeating pattern.

28. The method of claim 27 wherein the at least one analysis medium is a data line.

29. The method of claim 27 wherein the at least one analysis medium is an address line.

30. The method of claim 27 wherein the at least one analysis medium is a control line.

31. The method of claim 1 wherein the receive repeating pattern is repeated with a first period and the transmit repeating pattern is repeated with a second period, the first period and the second period bearing a multiple and submultiple relationship to each other.

32. The method of claim 31 wherein the first period and the second period are equal.

33. The method of claim 31 wherein the step of comparing the transmit repeating pattern and the receive repeating pattern is performed over multiple instances of the first period and the second period.

34. The method of claim 33 wherein the step of adjusting the parameter occurs in the transmit circuit.

35. The method of claim 33 wherein the step of adjusting the parameter occurs in the receive circuit.

36. The method of claim 35 wherein the parameter affects reception of a receive data input signal, the receive data input signal communicated along a first medium used to transmit the transmit repeating pattern to the receive circuit.

37. The method of claim 36 wherein the parameter further affects reception of a second receive data input signal, the second receive data input signal communicated along a second medium, the second medium being distinct from the first medium.

38. The method of claim 1 wherein the step of generating the transmit repeating pattern is performed so that the transmit repeating pattern is clocked at a transmit clock rate and the step of generating the receive repeating pattern is performed so that the receive repeating pattern is clocked at a receive clock rate, the transmit clock rate and the receive clock rate bearing a multiple and submultiple relationship to each other.

39. The method of claim 1 further comprising the step of:

adjusting a second parameter affecting reception of the transmit repeating pattern at the receive circuit.

40. The method of claim 39 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern comprises the step of:

comparing over a first range of the parameter and a second range of the second parameter.

41. The method of claim 1 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern comprises the step of:

detecting non-repeatability in a relationship between the transmit repeating pattern and the receive repeating pattern.

42. The method of claim 41 wherein the step of adjusting the parameter further comprises the step of:

adjusting the parameter based on the non-repeatability.

43. The method of claim 1 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison is performed at system start-up.

44. The method of claim 1 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison is performed upon detection of a communication failure.

45. The method of claim 1 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison is performed occasionally between periods of communication of user data between the transmit circuit and the receive circuit.

46. The method of claim 1 wherein the transmit circuit and the receive circuit are located within the digital signaling system being evaluated.

47. The method of claim 1 wherein the transmit circuit is located external to the digital signaling system being evaluated.

48. The method of claim 1 wherein the receive circuit is located external to the digital signaling system being evaluated.

49. A transmit circuit comprising:

a transmit data storage element adapted to receive data from a transmit data input to be sequentially transmitted as a transmit data output signal when the transmit circuit is operating in a normal mode, the transmit data storage element further adapted to provide a repeating pattern signal when the transmit circuit is operating in a test mode, the transmit circuit sequentially transmitting the transmit data output signal based on the repeating pattern signal when the transmit circuit is operating in the test mode.

50. The transmit circuit of claim 49 wherein the transmit data storage element comprises a shift register.

51. The transmit circuit of claim 49 further comprising:

a test loop coupled to the transmit data storage element when the transmit circuit is operating in the test mode, the test loop providing feedback to allow the transmit data storage element to provide the repeating pattern signal.

52. The transmit circuit of claim 49 wherein the repeating pattern signal has a data length greater than a data capacity of the transmit data storage element.

53. The transmit circuit of claim 49 wherein the repeating pattern signal represents a sequence of data bits, the transmit data storage element storing each of the data bits.

54. The transmit circuit of claim 49 wherein, when the transmit data storage element is divided into transmit data storage sub-elements during operation in the normal mode, the transmit data storage sub-elements are combined as the transmit data storage element for providing the repeating pattern signal when the transmit circuit is operating in the test mode.

55. The transmit circuit of claim 49 wherein the transmit data storage element is loaded from the transmit data input to initialize the test mode.

56. The transmit circuit of claim 49 wherein the transmit data storage element is loaded from a source other than the transmit data input to initialize the test mode.

57. The transmit circuit of claim 49 wherein the transmit data storage element is loaded via a parallel transmit load input.

58. The transmit circuit of claim 49 wherein the transmit circuit receives an adjustment signal from a receiver circuit, the receive circuit receiving the transmit data output signal, the transmit circuit adjusting a parameter of the transmit data output signal based on the adjustment signal.

59. The transmit circuit of claim 58 wherein the receive circuit is embodied in a first memory device and a second receive circuit is embodied in a second memory device.

60. The transmit circuit of claim 59 wherein the transmit circuit adjusts the parameter to a first value for communication with the first memory device and to a second value for communication with the second memory device.

61. A receive circuit comprising:

a receive data storage element adapted to output a receive data output signal based on a receive data input signal received at a receive data input when the receive circuit is operating in a normal mode, the receive data storage element further adapted to provide a repeating pattern signal when the receive circuit is operating in a test mode, and;

a comparison element, the comparison element adapted to perform a comparison of a relationship between the repeating pattern signal and the receive data input signal received at the receive data input and to produce a comparison output signal based on the comparison when the receive circuit is operating in the test mode.

62. The receive circuit of claim 61 wherein the receive data storage element comprises a shift register.

63. The receive circuit of claim 61 further comprising:

a test loop coupled to the receive data storage element when the receive circuit is operating in the test mode, the test loop providing feedback to allow the receive data storage element to provide the repeating pattern signal.

64. The receive circuit of claim 61 wherein the repeating pattern signal has a data length greater than a data capacity of the receive data storage element.

65. The receive circuit of claim 61 wherein the repeating pattern signal represents a sequence of data bits, the receive data storage element storing each of the data bits.

66. The receive circuit of claim 61 wherein, when the receive data storage element is divided into receive data storage sub-elements during operation in the normal mode, the receive data storage sub-elements are combined as the receive data storage element for providing the repeating pattern signal when the receive circuit is operating in the test mode.

67. The receive circuit of claim 61 wherein the receive data storage element is loaded from the receive data input to initialize the test mode.

68. The receive circuit of claim 61 wherein the receive data storage element is loaded from a source other than the receive data input to initialize the test mode.

69. The receive circuit of claim 61 wherein the receive data storage element is loaded via a parallel receive load input

70. The receive circuit of claim 61 wherein the comparison element detects variation of the relationship between the repeating pattern signal and the receive data input signal received at the receive data input.

71. The receive circuit of claim 70 wherein the repeating pattern signal is repeated with a first period and the receive data input signal is repeated with a second period, the first period and the second period bearing a multiple and submultiple relationship to each other.

72. The receive circuit of claim 71 wherein the first period and the second period are equal.

73. The receive circuit of claim 71 wherein the comparison of the relationship between the repeating pattern signal and the receive data input signal is performed over multiple instances of the first period and the second period.

74. The receive circuit of claim 73 wherein the receive circuit communicates the comparison output signal to a source of the receive data input signal.

75. The receive circuit of claim 73 wherein the receive circuit adjusts a parameter affecting its reception of the receive data input signal based on the comparison output signal.

76. The receive circuit of claim 75 wherein the parameter affects reception of a second receive data input signal, the second receive data input signal being distinct from the receive data input signal.

5

77. A method for operating a transmit circuit to provide for evaluation of a digital signaling system comprising the steps of:

passing data to be transmitted through the transmit circuit when the transmit circuit is operating in a normal mode; and

generating a transmit repeating pattern in the transmit circuit when the transmit circuit is operating in a test mode.

78. The method of claim 77 wherein the step of generating a transmit repeating pattern in the transmit circuit further comprises the step of:

preloading an initialization pattern into the transmit circuit.

79. The method of claim 77 wherein the step of generating a transmit repeating pattern in the transmit circuit further comprises the step of:

uniting a plurality of pipeline structures within the transmit circuit into a transmit repeating pattern generator when the transmit circuit is operating in the test mode.

80. The method of claim 79 wherein the step of passing data to be transmitted through the transmit circuit further comprises the step of:

passing distinct data through each of the plurality of pipeline structures when the transmit circuit is operating in the normal mode.

81. The method of claim 77 further comprising the steps of:

receiving the data in a receive circuit when the transmit circuit is operating in the normal mode; and

receiving the transmit repeating pattern in the receive circuit when the transmit circuit is operating in the test mode.

82. The method of claim 77 further comprising the steps of:

receiving the data in a receive circuit when the transmit circuit is operating in the normal mode; and

receiving the transmit repeating pattern in a test receiver separate from the receive circuit when the transmit circuit is operating in the test mode.

83. A method for operating a receive circuit to provide for evaluation of a digital signaling system comprising the steps of:

passing receive data through the receive circuit when the receive circuit is operating in a normal mode; and

generating a receive repeating pattern in the receive circuit when the receive circuit is operating in a test mode.

84. The method of claim 83 wherein the step of generating a receive repeating pattern in the receive circuit further comprises the step of:

preloading an initialization pattern into the receive circuit.

85. The method of claim 83 wherein the step of generating a receive repeating pattern in the receive circuit further comprises the step of:

uniting a plurality of pipeline structures within the receive circuit into a receive repeating pattern generator when the receive circuit is operating in the test mode.

86. The method of claim 85 wherein the step of passing data to be transmitted through the receive circuit further comprises the step of:

passing distinct data through each of the plurality of pipeline structures when the receive circuit is operating in the normal mode.

87. The method of claim 83 further comprising the steps of:

transmitting the data to the receive circuit from a transmit circuit when the receive circuit is operating in the normal mode; and

transmitting a transmit repeating pattern to the receive circuit from the transmit circuit when the receive circuit is operating in the test mode.

88. The method of claim 83 further comprising the steps of:

transmitting the data to the receive circuit from a transmit circuit when the receive circuit is operating in the normal mode; and

transmitting a transmit repeating pattern to the receive circuit from a test transmitter separate from the transmit circuit when the receive circuit is operating in the test mode.